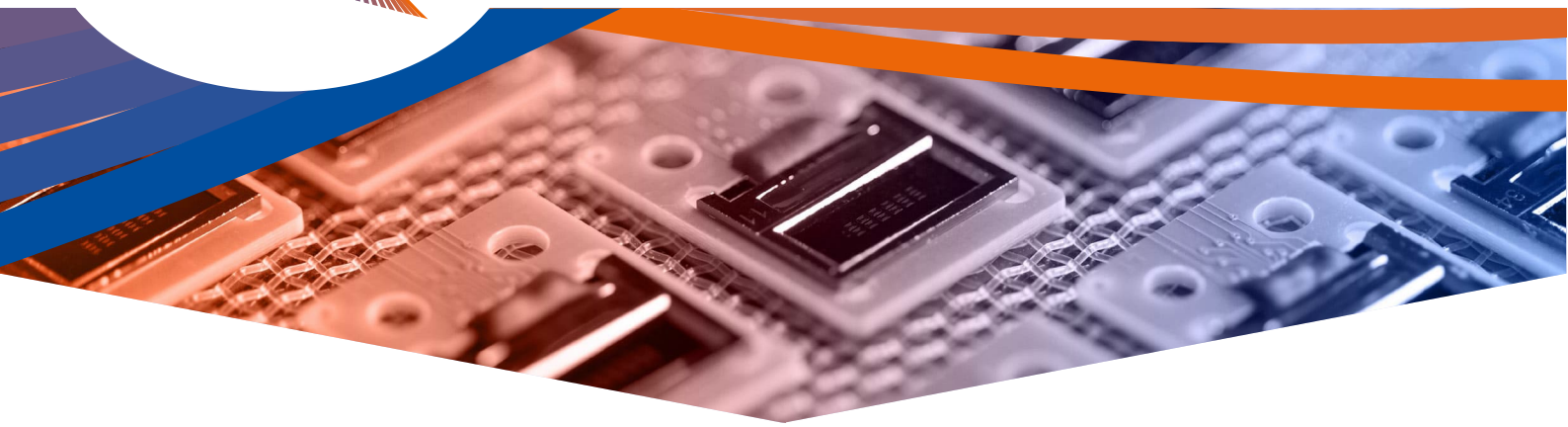
PHOTONICS ASSEMBLY

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

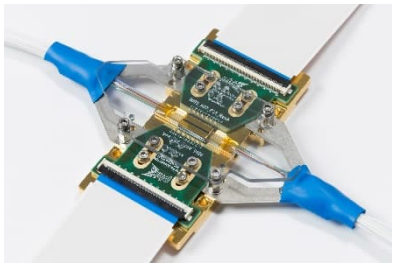
PHONE
+31 88 7449 000

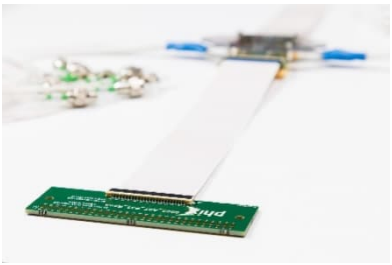
E-MAIL
sales@phix.com

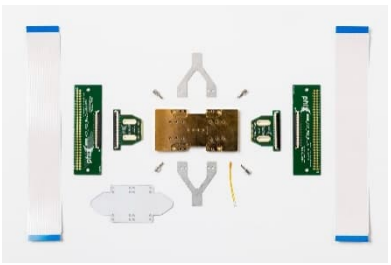


Design Rules for the PHIX Characterization Package

The PHIX Characterization Package is an open architecture packaging solution for photonic integrated circuits (PICs) of various sizes and material platforms. The package turns the PIC into an optoelectronic module by providing a housing with electrical connections, optical interfaces, and thermal management options. Adhering to the design rules outlined in this document allows PHIX to make use of standard off-the-shelf building blocks and deliver a cost-effective package at a short lead time while still providing significant flexibility.







Disclaimer and validity

- Please refer to the latest version of this document. The options and design rules may change over time and some configurations could become obsolete.
- After a document update, PIC designs based on an earlier version older than 3 years may be refused or be subject to additional charges.
- These design rules build on the PIC Design Guidelines document. Please read that first, since this provides more general background considerations for effectively laying out a chip for packaging.

Version management

v 1.3.1	January 2025	Modified DC bond pad placing rules, changed PCB nomenclature

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

Contents

1 Introduction

The PHIX Characterization Package is an open architecture packaging solution for photonic integrated circuits (PICs) of various sizes and material platforms. It provides optical interfaces, electrical connections, thermal management, and mechanical support for the PIC. Adhering to the design rules outlined in this document allows PHIX to make use of standard off-the-shelf building blocks and deliver a cost-effective package with a short lead time while providing significant flexibility.

If some customization is required, this can easily be added to the standard building blocks. However, any customization will quickly lead to much higher costs and longer lead-times due to the extra resources and/or non-recurring engineering. For prototype manufacturing, it is therefore recommended to avoid customization as much as possible. For volume manufacturing, on the other hand, PHIX would be happy to advise you on customized design optimizations that will lead to higher performance and lower costs in the long run.

PHIX will continue to expand its standard offering by working with PIC foundries and their platforms to further develop modular packaging solutions. Please check our website for the latest version of this document. Our PIC Design Guidelines cover more general basic design guidelines on which this document builds. They also provide more details on each packaging option discussed in this document and possible customizations that we can support.
Once you have selected a package type, please refer to our relevant Design Rules document for that package, if available. This document contains design rules specific to the PHIX Characterization Package.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

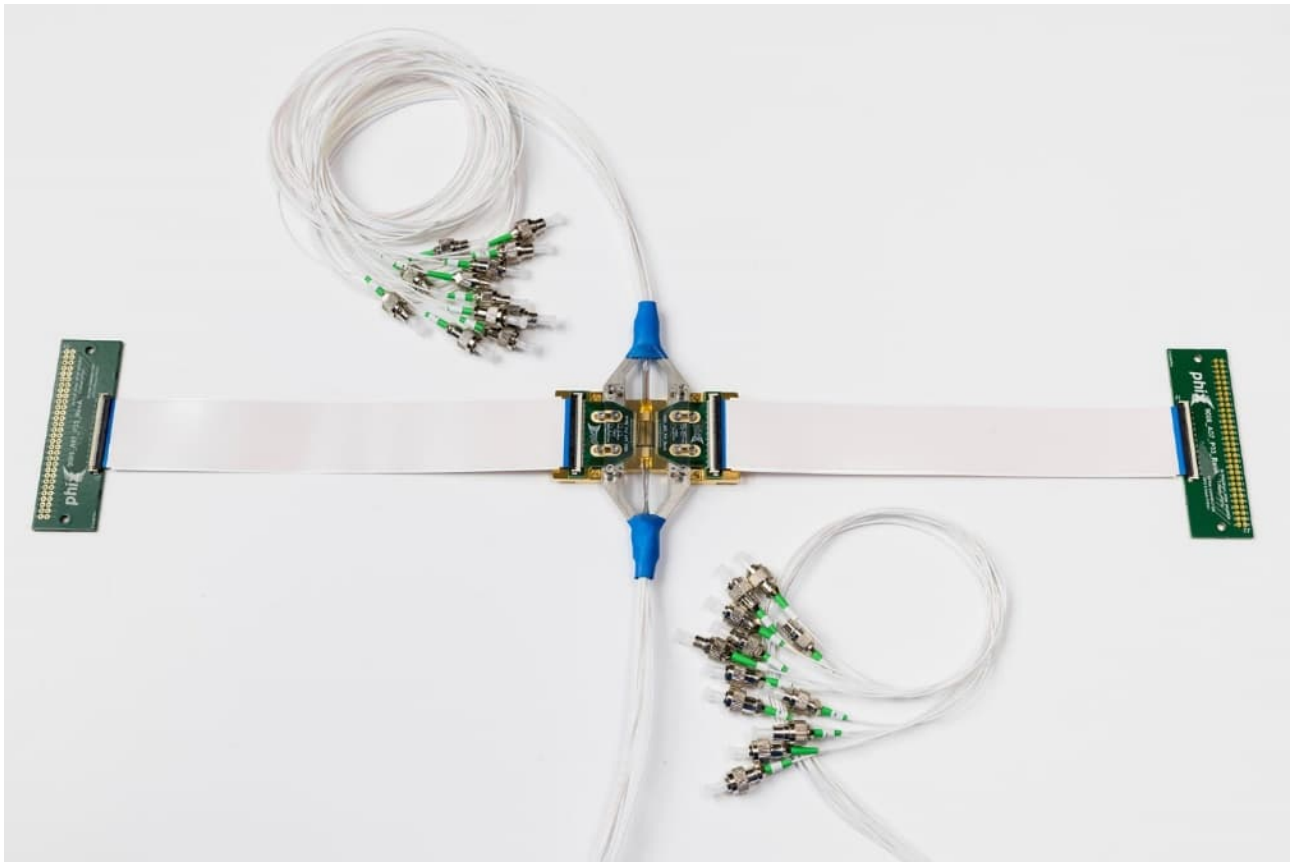


Figure 1: The PHIX Characterization Package

2 PHIX Characterization Package overview

2.1 Key features and benefits

Key features

- 4 to 20mm PIC sizes of several material platforms are supported.
- Electrical and optical interfaces:
  - Up to 2 optical (east/west)
  - Up to 2 electrical (north/south)
- Edge coupled and grating coupled optical fiber interfaces are supported.
- Up to 32 optical I/Os per side (see section 4.1 for number of functional waveguides).
- SM or PM fiber options with FC-APC connectors.
- Up to 2 fan-out printed circuit boards with 60 DC electrical contacts each.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

Benefits

- Packaging platform using cost-effective off-the-shelf building blocks for delivery with short lead times.
- Open architecture for easy chip and device characterization
- Robust package with fiber strain reliefs and transparent removable cover.
- Thermally stable with large gold-plated copper base with integrated thermistor for direct temperature feedback.
- Easily mountable on an optical table with the Cooling Carrier option, featuring a 20W thermoelectric cooler (TEC).

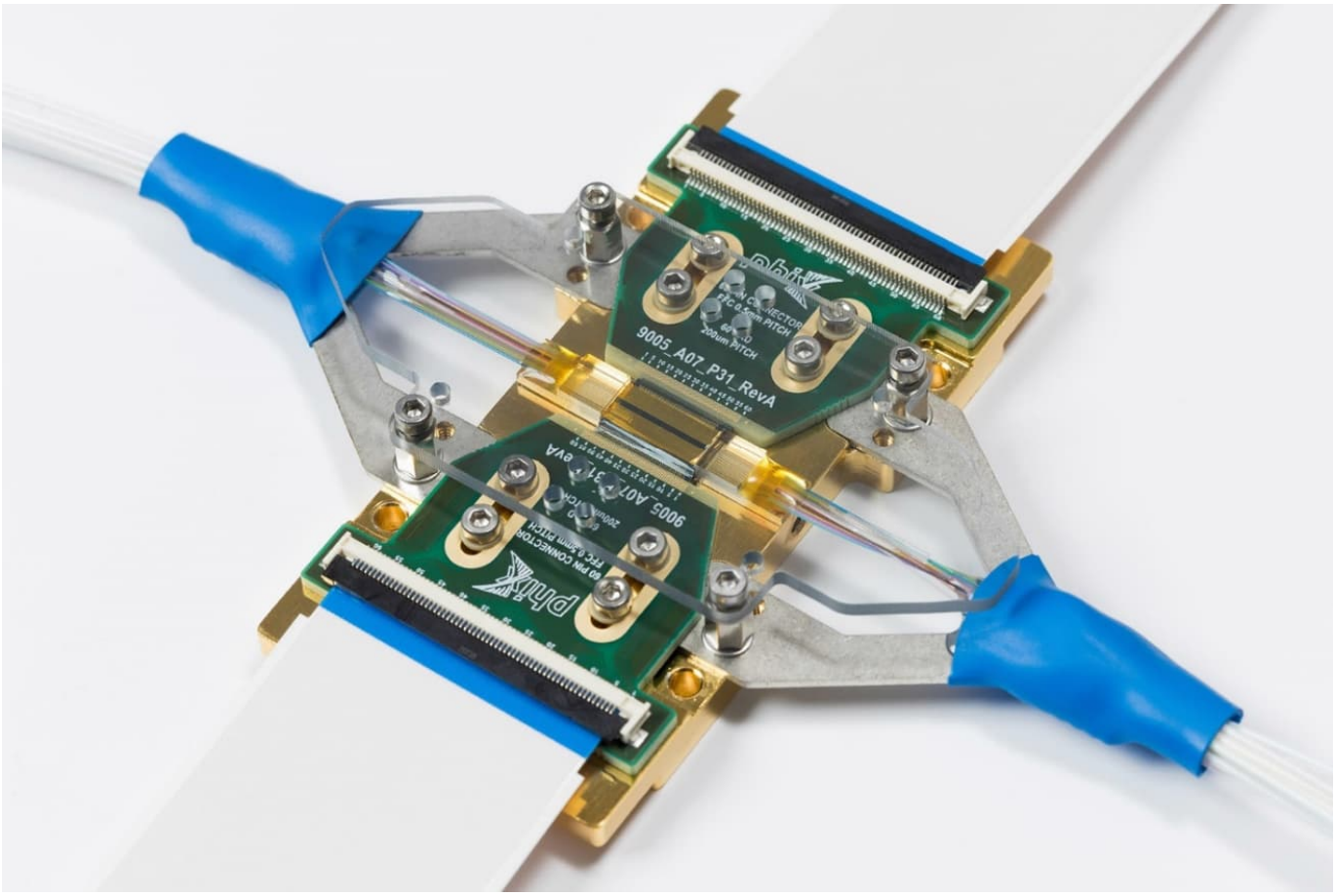


Figure 2: PHIX Characterization Package, close-up of main housing

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

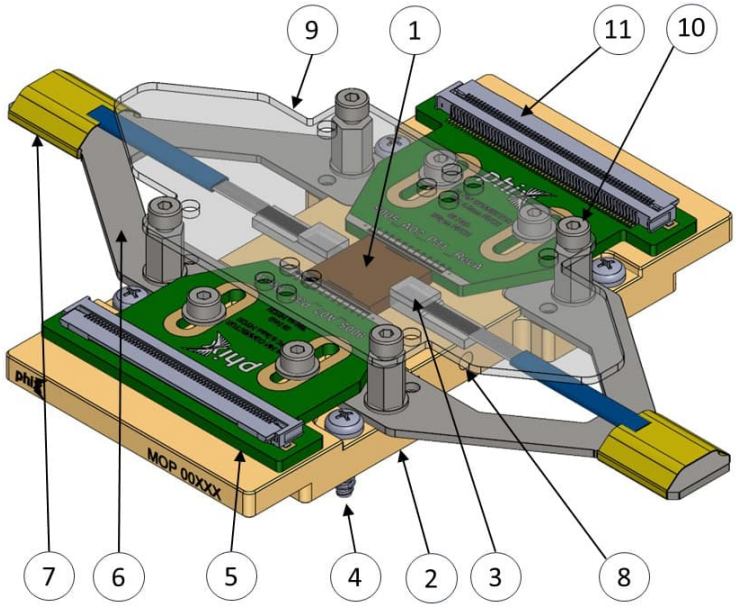
PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

2.2 Module layout

Legend

1. PIC
2. Gold-plated copper base
3. Fiber array
4. Base mounting screws
5. DC connector PCB
6. Strain relief
7. Shrink tube
8. Thermistor cavity
9. Module cover plate
10. Cover screw
11. 60-pin FFC connector
12. FFC cable
13. DC breakout PCB



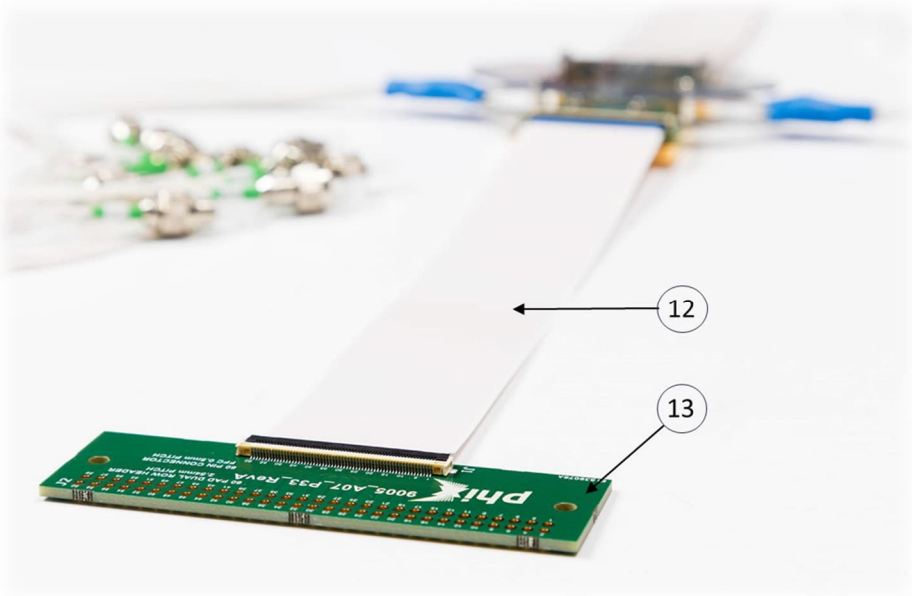


Figure 3: Components of the PHIX Characterization Package

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

2.3 Supported PICs

As a first step in deciding if the PHIX Characterization Package is the right fit for your project, please look at the supported PIC materials and PIC sizes. The following tables help clarify this.

	Supported
	Not supported
	Possibly supported, please ask PHIX

2.3.1 Supported material platforms

The PIC material platforms silicon nitride (SiN) and silicon photonics (SiPh, silicon on insulator) are supported in the standard PHIX Characterization Package. Indium phosphide (InP), thin film lithium niobate (TFLN), and hybrid solutions can also qualify, but require a 3D design check by PHIX as they do not follow a standard assembly process and additional process development may be necessary.
For SiPh please note that PHIX's standard offering currently only supports inverted tapers (see section 4.4.5 for guidelines). Suspended tapers require a custom solution.
If using InP, please look extra carefully at our requirements for chip dimensions (section 2.3.2), waveguide pitch, and waveguide angle (section 4.2).
We are happy to advise you about a custom modification or tailor-made packaging solutions.

Material platform	Standard PHIX Characterization Package	Custom PHIX Characterization Package	Other custom packaging solution
SiN			
SiPh			
TFLN			
InP			
Hybrid solutions			
Other materials			

Table 1: Supported PIC material platforms

If your PIC is of a different material, please contact PHIX to inquire whether it's a good fit for the PHIX Characterization Package.

2.3.2 Supported PIC dimensions

The dimensions of the PHIX Characterization Package standard building blocks are compatible with PICs with a minimum edge length of 4 mm and a maximum edge length of 20 mm, as indicated in table 2. This means that the smallest PIC size supported by the PHIX Characterization Package is 4 x 4 mm^2 and the biggest is 20 x 20 mm^2. Any rectangular sizes between these two extremes are also supported.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

PIC dimensions	Standard PHIX Characterization Package	Custom PHIX Characterization Package	Other custom packaging solution
Smallest edge ≥ 4mm and longest edge ≤ 20 mm			
Smallest edge ≥ 2.5 mm and longest edge ≤ 32 mm			
Other dimensions			

Table 2: Supported PIC dimensions

2.3 Optical coupling

2.3.1 Fiber array configurations

We can provide v-groove fiber arrays for edge coupling or quasi-planar grating coupling schemes. There can be fiber arrays on both sides of the module, just one, or none. Each side can have up to 32 channels, but please refer to section 4.1. to find out the maximum number of functional waveguides for your configuration. Standard supported fiber pitches are 127 or 250 µm, with a flat or angled polished interface.

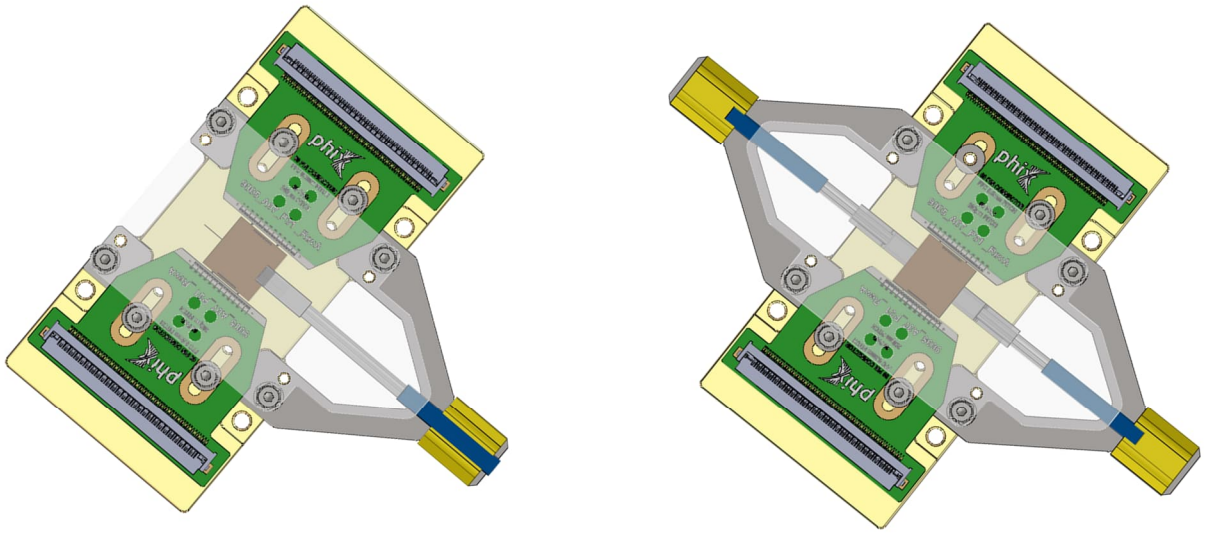


Figure 4: PHIX Characterization Package with single sided grating coupling (left) and with double sided edge coupling (right)

2.3.2 Supported fibers and polarization

For the PHIX Characterization Package we support SMF28 single mode (SM) fiber and PM1310 or PM1550 polarization maintaining (PM) fiber. The table below shows the compatible wavelength range for these fibers. Many other fiber types covering a wavelength range from 400 to 2300 nm are available as part of custom configurations.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

Our standard configuration allows you to use an array of one fiber type on one side of the PIC and an array of another fiber type on the other. However, mixing fiber types within a single fiber array is only possible in a custom configuration.

Fiber name	Wavelength range (nm)		Fiber type
	Min	Max	
SMF28	1270	1625	SM
PM1310	1260	1360	PM
PM1550	1500	1600	PM

Table 3: Standard fiber options for the PHIX Characterization Package

If a PM fiber is used, then it's important to align the polarization (rotation) of the fiber properly to the waveguide. For our standard PHIX Characterization Package we offer a horizontal (H) polarization coupling to the PIC waveguide.

Figure 5: Supported fiber array polarization

2.3.3 Fiber cables and connectors

The fiber array cables supplied with the PHIX Characterization Package have a buffer of 900 µm, a length of 1 meter, and are fitted with fiber numbering labels for your convenience. The connectors are FC-APC type with slow axis to key polarization, as shown in figure 6 below.

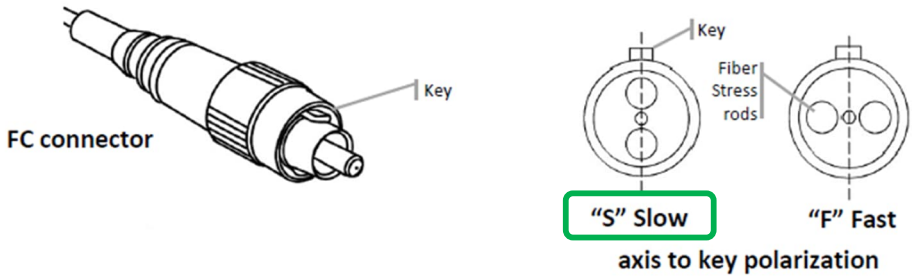


Figure 6: Slow polarization aligns the stress rods with the connector key

Fiber cables of other lengths and with different connectors are available as custom configurations. Please contact PHIX for further information.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

2.3.4 Spot size converters

Spot size converters (SSC) can be attached to fiber arrays to reduce the mode field mismatch between the fibers and the PIC waveguides. They are standard options for the PHIX Characterization Package. Whether or not they would benefit your project depends on the mode field diameter (MFD) of your PIC waveguides (see section 4.3) and the acceptable optical insertion losses for your project. PHIX can determine this together with you.

Mode field matching is also possible using ultra-high numerical aperture (UHNA) fibers. This is supported by PHIX as a custom option.

More information about PHIX spot size converters can be found in our SSC white paper.

2.4 Electrical connections

The PHIX Characterization Package supports the fan-out of up to 60 DC bond pads on each side of the PIC. The DC connector printed circuit boards (PCBs) distribute the signals to 60 pin Molex FFC/FPC connectors, to which the provided additional DC breakout PCBs can be connected through flat flex cables (FFCs).

Figure 7: DC breakout PCB

A possible custom option would be to designate the west side of the PIC to DC electrical I/O if no fiber array is needed there. Please contact PHIX to discuss the possibilities.
If your PIC requires connectivity with radio frequency (RF) signals, then the PHIX RF Characterization Package would be a better choice.

2.5 Thermal management

The PHIX Characterization Package is designed to be able to manage the thermal behavior of the PIC. The silicon or aluminum nitride submount on which the PIC is placed dissipates the heat to a gold-plated copper base. Inside this base is a cavity with a 10kΩ negative temperature coefficient (NTC) thermistor, with which the temperature of the module can be measured.

The PHIX Cooling Carrier is an optional expansion for the PHIX Characterization Package that allows the temperature to be regulated using a 20W thermoelectric cooler (TEC). The Cooling Carrier is attached below the module and has a convenient mounting plate for connection to an optical table. Using a TEC controller (not included) the temperature of the PIC can be kept at a constant value. More information on this can be found on the PHIX Cooling Carrier web page.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

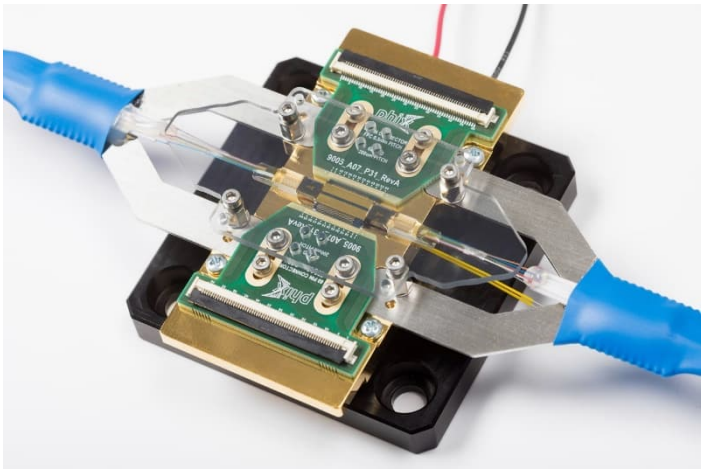


Figure 8: PHIX Characterization Package with a PHIX Cooling Carrier mounted underneath

If you require the integration of the TEC element directly under the PIC, please contact PHIX for a custom solution.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

3 General design rules

3.1 PIC orientation and naming convention

It is a common standard within integrated photonics to use the north, south, east, and west naming for the various PIC edges as shown in figure 9. PHIX uses the west and east sides for the optical interfaces, with east (FA) being the primary interface for fiber arrays. The north and south are reserved for electrical (DC) bond pads.

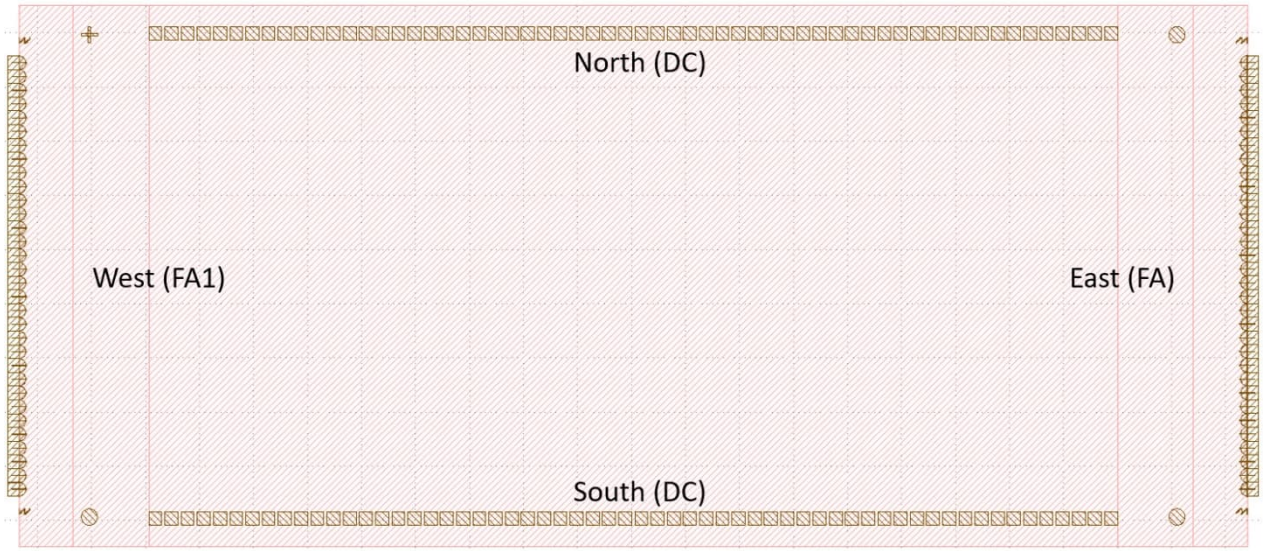


Figure 9: Definition of PIC orientation

Basic layout rules:

- All optical interfaces are west and east
- All electrical interfaces are north and south

Custom solutions can also have electrical connections (DC or RF) at the east side, if only one fiber array is used. Please contact PHIX for further information if this is required.

3.2 PIC fiducial markings

To facilitate assembly and automation PHIX uses fiducial markers to identify the orientation of the PIC. For the assembly of our PHIX Characterization Package we request the following markings:

- Chip orientation markers (waveguide layer and/or metal layer)
  - One 150 x 150 µm^2 equal-armed cross at the northwest corner and three circles with 150 µm diameter in all other corners. All located at least 200 µm from the north/south edges and at least 75 µm from the epoxy keep-out zone E. The value of E is different for an edge coupling and grating coupling configuration, respectively 500 µm and 1250 µm (see sections 4.4.2 and 4.5.3 for more details).
- Fine rulers for chip polishing (waveguide layer)
  - A ruler close (but with a minimal clearance of 300 µm from the electrical edge) to each corner, at least at each optical I/O side.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

- Each ruler with 5 µm divisions from at least 0 to -100 µm (see figure 11).
- The optimum fiber core coupling point should be positioned in the range of 0 to -30 µm.
- The ruler must be aligned to the chip edge depending on the specific foundry design rules

A sample GDS file is available from PHIX on request.

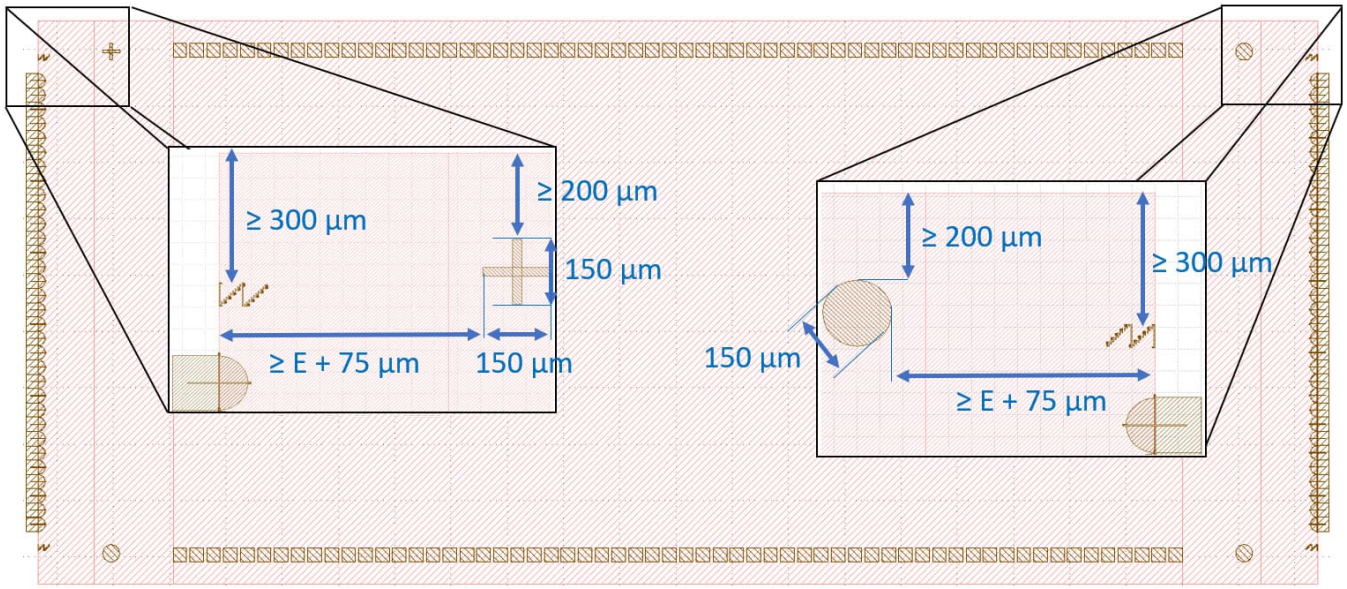


Figure 10: Overview of the markings

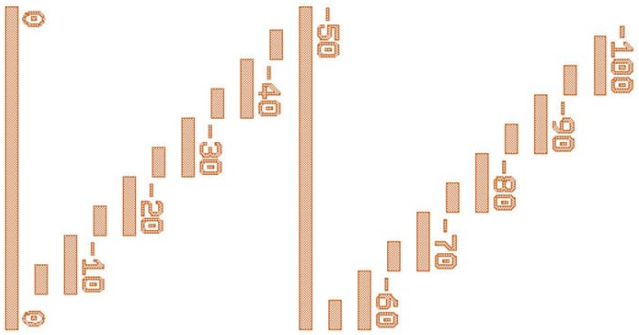


Figure 11: Polishing ruler details

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

3.3 PIC dicing

You can deliver your PICs to PHIX in the following states:

1. On a wafer, with no dicing or etching having been performed. PHIX will do the dicing (as a separate service, not covered in the price of the PHIX Characterization Package). Please note that PHIX cannot perform cleaving of InP wafers.
2. Diced or cleaved by the PIC foundry.
3. Etched all the way through at the optical interfaces.
4. With a deep trench at the optical interfaces to expose the waveguides.

If a deep trench is combined with an inverted waveguide taper at the optical interface, please refer to section 4.4.4 for special instructions.
For dicing clearances to bond pads at the PIC edges, please refer to section 5.2.

4 Optical design rules

4.1 Number of functional waveguides

The standard offering of the PHIX Characterization Package with off-the-shelf building blocks is based on a selection of standard fiber arrays and spot size converters (SSCs) that we keep in stock. This selection of components determines the maximum number of functional waveguides that you can use on the PIC in order to benefit from this standard offering. This number is based on our use of waveguide alignment loops (see sections 4.4.1 and 4.5.2) and the option of using a spot size converter (see sections 2.3.4 and 4.3).

The following table shows the maximum number of (functional) waveguides per optical interface depending on fiber coupling scheme and the use of an SSC.

Fiber coupling scheme	Max. fibers per side		Max. waveguides per side		Max. functional waveguides per side	
	127 µm pitch	250 µm pitch	127 µm pitch	250 µm pitch	127 µm pitch	250 µm pitch
Grating coupling	32	12	32	12	30	10
Edge coupling	32	12	32	12	28	8
Edge coupling with SSC	32	12	28	8	24	4

Table 4: Number of functional waveguides per optical interface

4.2 Waveguide alignment, pitch, power limit, and angle

The waveguides at the optical interface should be centered on the PIC edge, so that the fiber array can be placed in the middle of the facet. The pitch of the waveguides should match that of our available fiber arrays. Our v-groove fiber arrays can have a pitch of 127 µm or 250 µm.

The optical interface power limit per channel is 20 dBm (100 mW) at 1550 nm with a 10 µm mode field diameter (MFD). A higher optical power, lower wavelength, and/or smaller MFD may degrade the index matching epoxy present at the optical interface between fiber array and PIC.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

We do not support angled waveguides for our standard configuration. If angled waveguides are required for your application, please contact PHIX for a custom solution.

4.3 Mode field matching

The optical fibers supported by the PHIX Characterization Package are listed again in the table below, this time including their mode field diameters (MFDs). If possible, make sure you match these MFDs as closely as possible in the waveguides at the PIC facet, for example by using an inverted taper (on-chip spot size converter).

	Wavelength (nm)		Fiber type	MFD (µm, ± 0.5 µm)	
	Min	Max		@ 1310 nm	@ 1550 nm
SMF28	1270	1625	SM	9.2	10.4
PM1310	1260	1360	PM	9.0	n/a
PM1550	1500	1600	PM	n/a	10.5

Table 5: Wavelengths and mode field diameters of the standard fiber types

If, in edge coupling configurations, a mode field mismatch remains, then PHIX can place spot size converters (SSCs) between the fiber array and the PIC. These building blocks convert the fiber MFD down to a circular PIC mode field between 5x5 µm and 1.5x1.5 µm, or an oval mode field between 5x1 µm and 1.5x1 µm. PHIX will discuss with you the optimal trade-off between performance and cost that comes with the inclusion of these SSCs.

Please note that if SSCs are used then the strain reliefs provided with the package will be longer.

As an alternative to the use of PHIX SSCs, mode field matching is also possible using ultra-high numerical aperture (UHNA) fibers. This is supported by PHIX as a custom option.

4.4 Edge coupling design rules

4.4.1 Alignment loops

Alignment loops are critical for standardizing assembly. The cost of the extra fibers in the fiber array and loops on the PIC are much lower than handling each PIC as a custom alignment project in low volume.
For edge coupling two loops (4 extra waveguide I/Os) are required, one on each side of the fiber array.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

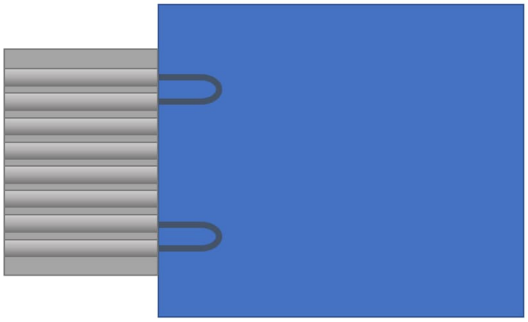


Figure 12: Alignment loops required for edge coupling of fiber arrays to a PIC

4.4.2 Keep-out area

To allow for proper assembly there should be no waveguides any closer than 450 µm to the north and south sides of the PIC.

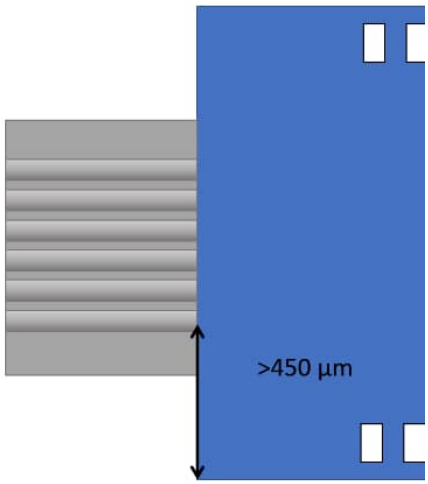


Figure 13: Waveguide to edge keep-out area for edge coupling

During the fiber array assembly process some epoxy may flow out onto the PIC surface, in the orange area shown below. Do not place structures on the chip within this area that may not function properly if covered with epoxy.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

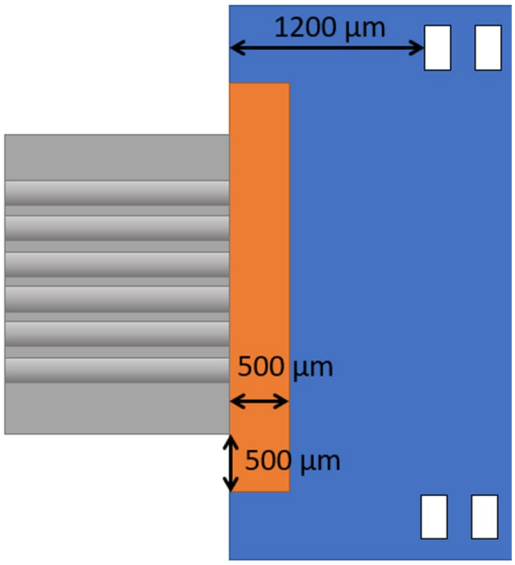


Figure 14: Space reserved for adhesive fillets in an edge coupling configuration

4.4.3 0-degree or 8-degree coupling

The standard configuration for the PHIX Characterization Package is a 0° or 8° polishing angle between the fiber array (or SSC) and the PIC. An 8° polishing angle offers reduced back reflection losses at the interface. This 8° option is not available for InP PICs.

Figure 15: Angled polishing of the fiber-to-chip interface

4.4.4 Deep trench with inverted taper for SiPh edge couplers

If a deep trench is combined with an inverted waveguide taper at the optical interface of the SiPh PIC, then PHIX has a special instruction that will allow us to polish the optical facet without compromising the taper.

PHIX requires a waveguide section of fixed size and constant target MFD, located before the start of the actual taper. This waveguide section should be at least 30 µm long, corresponding to the polishing landing area (between 0 and -30 µm, see section 3.2). Our polishing process will remove material to get as close as possible to the -30 µm marker, but not go beyond.

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PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

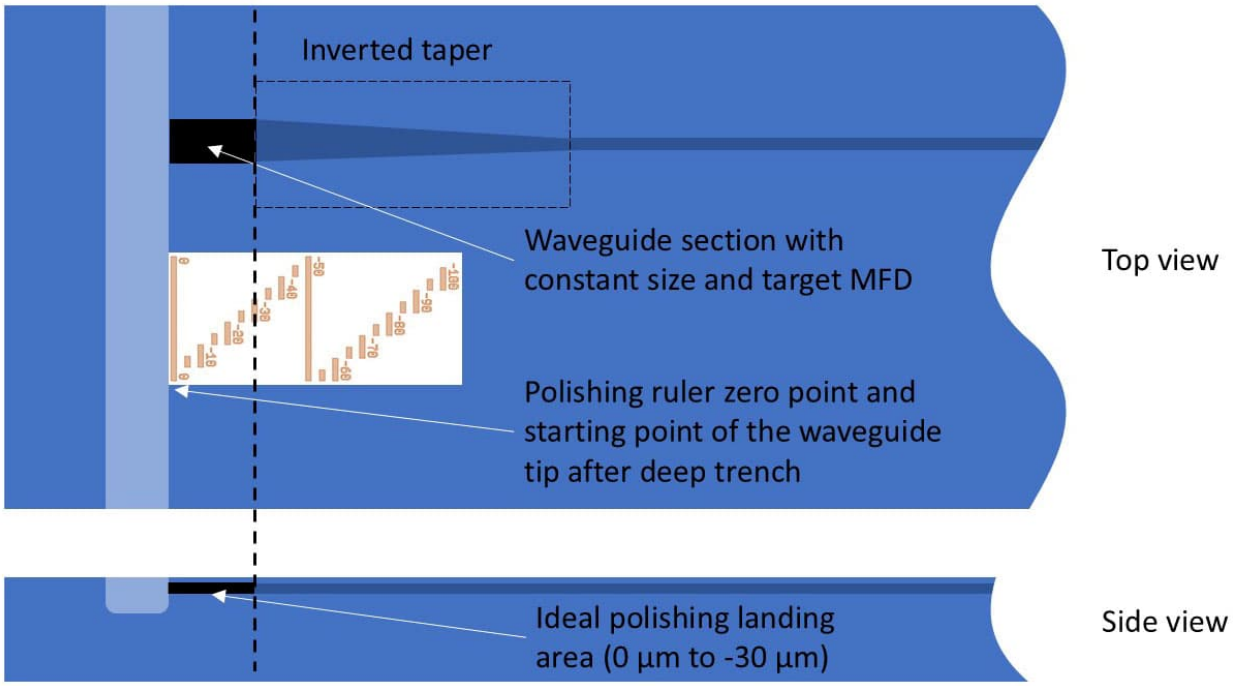

Figure 16: Extended waveguide after inverted taper

4.5 Grating coupling design rules

4.5.1 Grating location

For grating coupling PHIX uses a quasi-planar configuration with recessed lid fiber arrays. The location of the grating coupler structure needs to be between 750 and 800 µm from the PIC edge to allow for a good mechanical connection between the fiber array and the PIC. The fiber arrays have a 12-degree coupling angle in air that needs to match the PIC exit angle from the grating in air.

Figure 17: Quasi-planar grating coupling for the fiber-to-chip interface

4.5.2 Alignment loops for grating coupling

Alignment loops are critical for standardizing assembly. The cost of the extra fibers in the fiber array and loops on the PIC are much lower than handling each PIC as a custom alignment project in low volume.

One advantage of grating couplers compared to edge couplers is that alignment is less strict. Hence, to facilitate good alignment for a grating coupling configuration, PHIX requires only one alignment loop (2 extra waveguide I/Os) between the first and last fiber in the fiber array.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

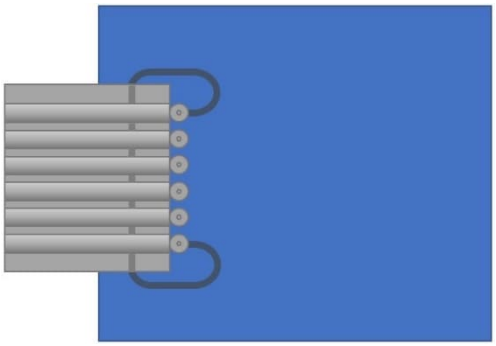

Figure 18: Single alignment loop for grating coupled fiber array

4.5.3 Keep-out areas for grating coupling

To allow for proper assembly there should be no waveguides any closer than 450 µm from the north and south sides of the PIC.

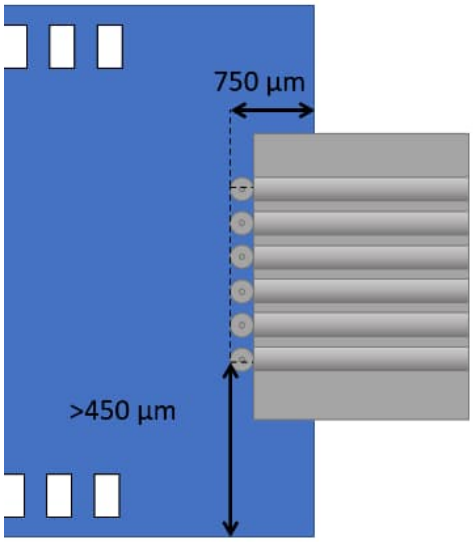

Figure 19: Waveguide to edge keep-out area for grating coupling

During fiber array assembly process some epoxy may flow onto the PIC surface, in the orange area shown below. Do not place structures on the chip within this area that may not function properly if covered with epoxy.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

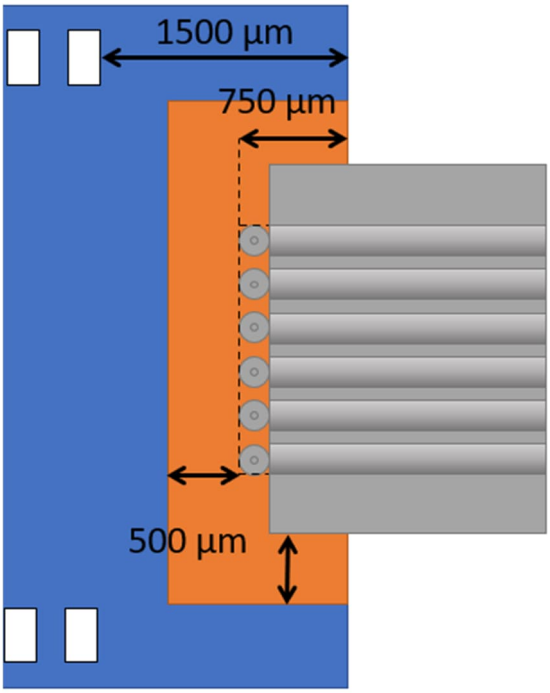

Figure 20: Space reserved for adhesive fillets by grating coupling

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

5 Electrical interface design rules

The PHIX Characterization Package supports DC electrical connections at the north and south PIC edges. We use wire bonding with 17.5 µm gold wire to distribute the electrical signals to PCBs and 60-pin FFC connectors.

5.1 General bond pad rules

- Number of pads per side: ≤ 60
- Pad surface finish: gold (Au) or aluminum (Al)
- Current per pad: ≤ 200 mA (if wire bond length can be kept below 1.5 mm)

5.2 Bond pad size and locations

- Bond pad arrangement: inline, centered between the PIC's east and west edges
- Bond pad size: width and length of 120 µm +/- 30 µm, equal for all pads
- Bond pad pitch: 200 µm +/- 50 µm
- Distance of bond pad to PIC edge: ≥ 100 µm and ≤ 500 µm

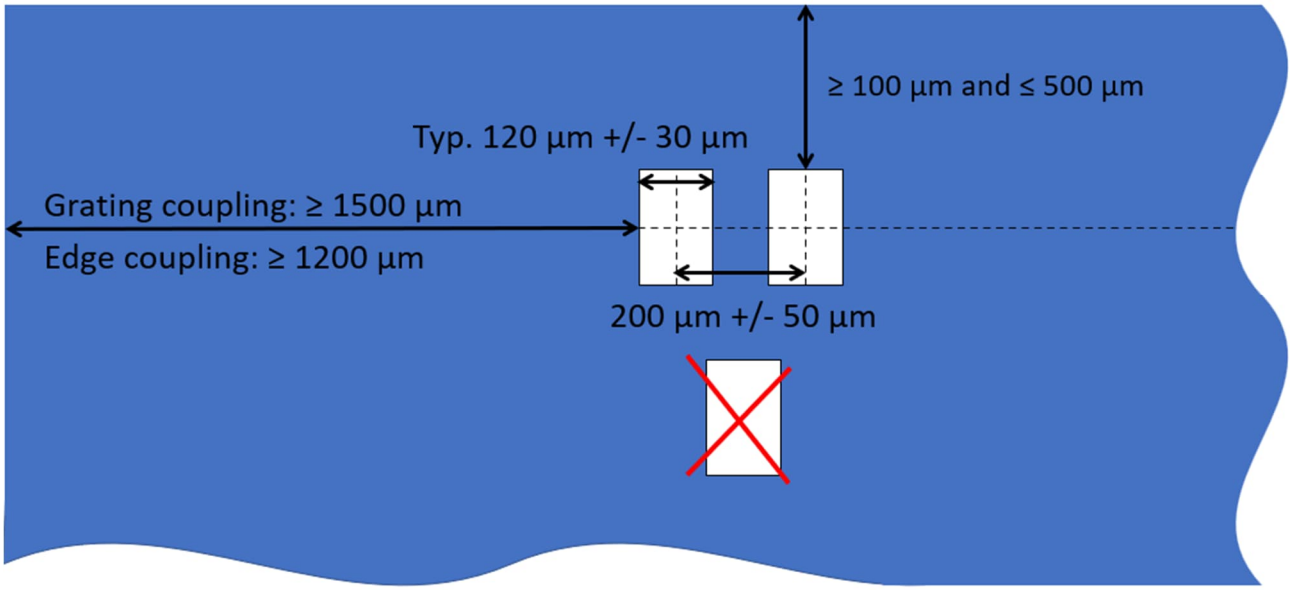

Figure 21: Bond pad dimensions and placement rules

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

- Keep-out area from side edges for edge coupling (EC): ≥ 1200 µm
- Keep-out area from side edges for grating coupling (GC): ≥ 1500 µm

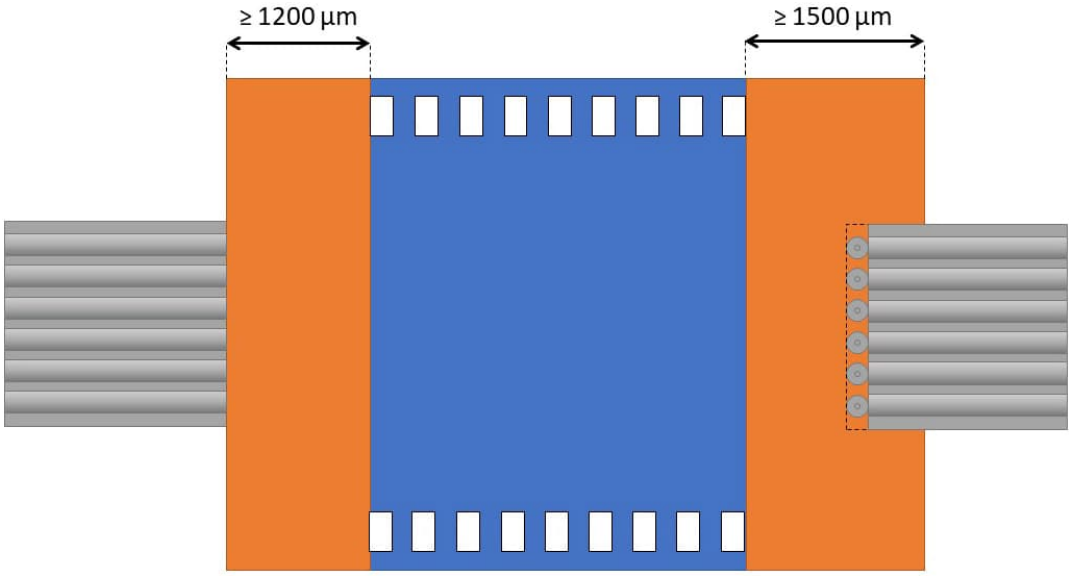

Figure 22: DC-bond pad keep-out areas for edge coupling and grating coupling

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

6 Design rules checklist

	PIC Parameters	Unit	Specification for standard PHIX Characterization Package 1.5		Comply?
PIC dimensions	PIC size max. [width, length]	mm	W=20, L=20		□
	PIC size min. [width, length]	mm	W=4.0, L=4.0		□
Optical interfaces	Fiber type		SMF28, PM1310 or PM1550		□
	Wavelength range	nm	1270-1625 (SMF28), 1260-1360 (PM1310) or 1500-1600 (PM1550)		□
	Optical power per channel [max]	mW @1550	100		□
	PIC MFD [min (x,y), max (x,y)]	µm	min (1.5, 1.0), max (10.5, 10.5)		□
	Waveguide I/O pitch	µm	127 or 250		□
	Waveguide I/O channel count per side [max]	#	32 (for 127 µm pitch) or 12 (for 250 µm pitch)		□
	Fiber coupling scheme		Edge coupling	Grating coupling	
	Waveguide channels reserved for alignment loops	#	4	2	□
	Waveguide I/O to PIC edge [min/max]	µm	0/30	750/800	□
	Waveguide I/O to sides clearance [min]	µm	450	450	□
	Epoxy keep-out zone (from waveguide I/O area)	µm	500	500	□
	Waveguide exit angle	°	0 (±0.5)	12 (±1)	□

CONTACT
PHIX B.V.
Hengelosestraat 525
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The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

DC interfaces	Electrical DC connections per side [max]	#	60	☐
	Bond pad arrangement (centered)		In-line, single row, centered	☐
	Bond pad surface finish		Gold or aluminum	☐
	Bond pad keep-out area from sides [min]	µm	1200 (edge coupling) or 1500 (grating coupling)	☐
	Bond pad pitch	+/-50 µm	200	☐
	Bond pad dimensions	+/-30 µm	120 by 120	☐
	Bond pad to PIC edge [min]	µm	100	☐
	Bond pad to PIC edge [max]	µm	500	☐
	Current per channel [max]	mA	200	☐
Marker fiducials	PIC markers at corners	Waveguide and/or metal layer	1 cross (northwest) and 3 circles (other corners)	☐
	Polishing rulers (for edge coupling only)	Waveguide layer	At each side of the waveguide I/O area (5 µm per division)	☐

Table 6: Design rules checklist

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

Appendix A: Specifications

A.1 Standard specifications

	Module Parameters	Unit	Specification for standard PHIX Characterization Package
General	Size module max (outer)	mm	107.5 x 47.0 x 14.6
Optical coupling	Connector		FC-APC
	Fiber length	m	1
	Optical power per channel [max]	mW @1550	100
DC interface	Connector		2x 60-pin connector for FFC
DC wire bonding	Wire diameter	µm	17.5
	Wire material		Au
	Current per channel [max]	mA	200
Thermal	TEC (optional Cooling Carrier) power [max]	W @RT	20
	NTC Thermistor resistance	kOhm	10 ($B_{25/85}$ 3977K)

Table 7: PHIX Characterization Package standard specifications

A.2 Outer dimensions and mounting options

The basic dimensions of the module can be found below. Also indicated are the mounting holes for M2.5 screws that can be used to attach the module to a table, box, or cold plate.
Please note that if spot size converters are used (see section 4.3) then a longer variety of strain reliefs is used compared to the ones pictured below. The longer strain relief is 60 mm long while the short one is 42 mm long. A PHIX Characterization Package with two strain reliefs of the longer variety will therefore have a length of 143.5 mm.

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

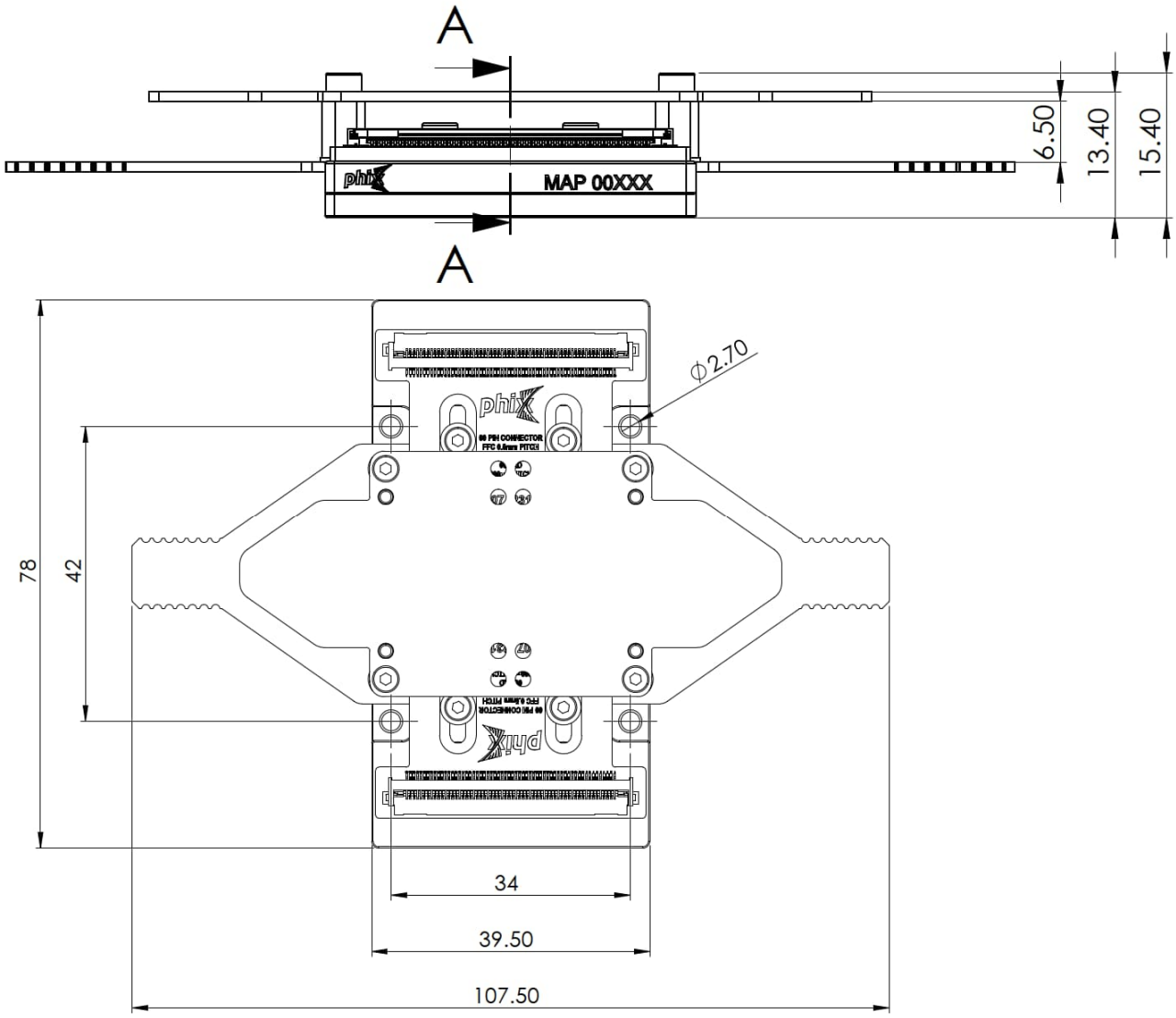

Figure 23: PHIX Characterization Package module dimensions (in mm)

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

A.3 Flex cable and connector specifications

	Manufacturer	Product Number	Description	Details
Connector	Molex	5051106091	CONN FFC BOTTOM 60POS 0.5MM R/A	60 Position FFC, FPC Connector Contacts, Bottom 0.020" (0.50mm) Surface Mount, Right Angle
Flex cable	Molex	150180571	FFC NOTCH 60 CIRC A 203MM	0.50mm Pitch Premo-Flex FFC Jumper with Ears, Same Side Contacts (Type A), 203.00mm Cable Length, Gold (Au) Plating, 60 Circuits

Table 8: Flex cable and connector specifications

A.4 DC breakout PCB dimensions

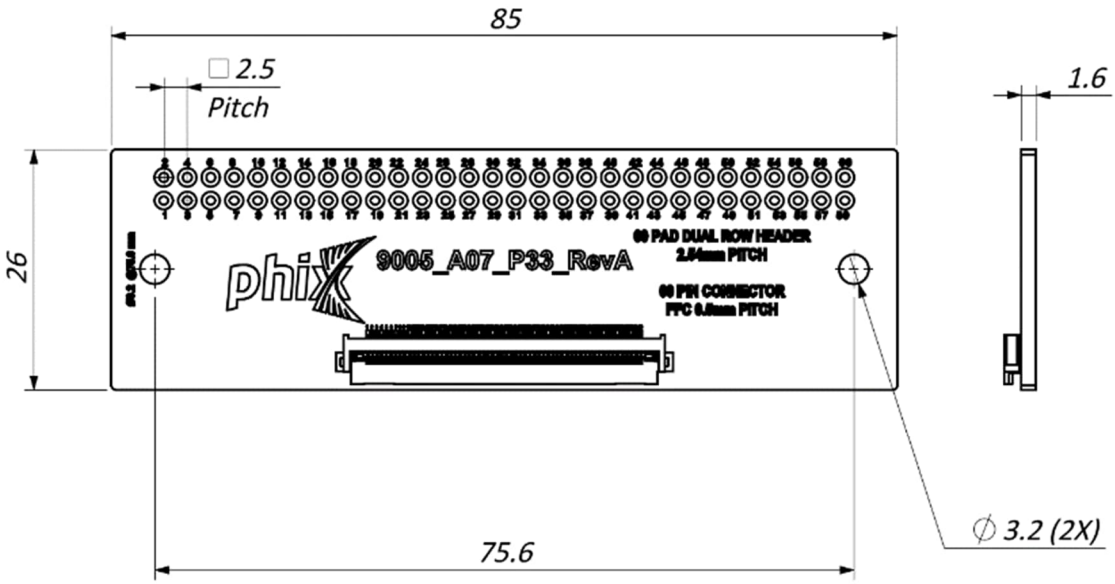

Figure 24: DC breakout board dimensions (in mm)

CONTACT
PHIX B.V.
Hengelosestraat 525
7521 AG Enschede
The Netherlands

PHONE
+31 88 7449 000

E-MAIL
sales@phix.com

Appendix B: PIC layout Template (GDS)

A template for the PHIX Characterization Package is available in GDS format to indicate the preferred location of the optical and electrical I/O, as well as the location of the markers that are required on the PIC. The red markers can directly be used in your own design and are also available as separate GDS files. You can find the GDS files on our download page.

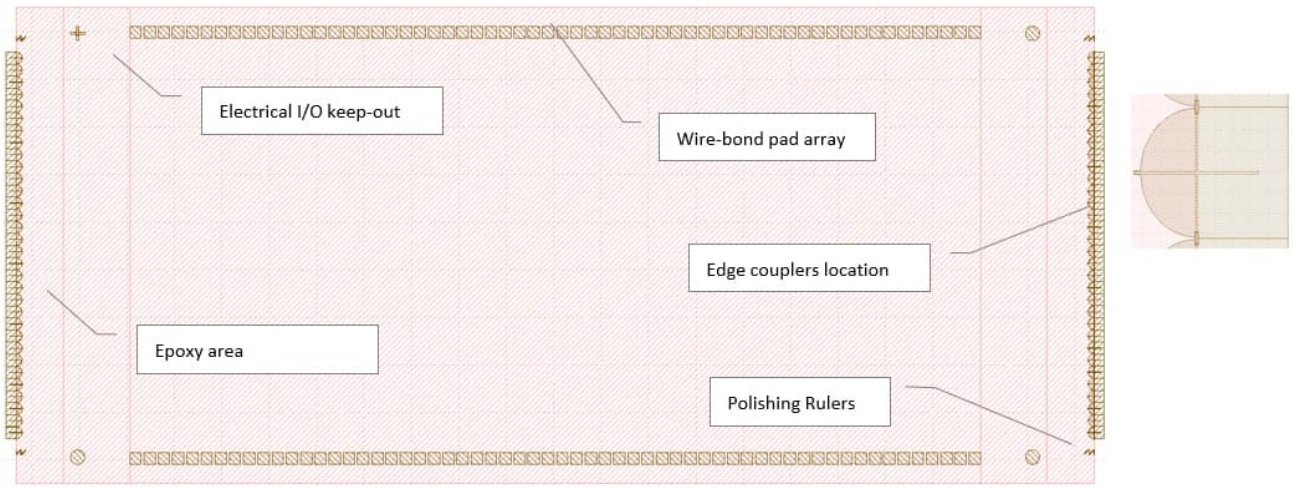

Figure 25: Example of a GDS file for edge coupling

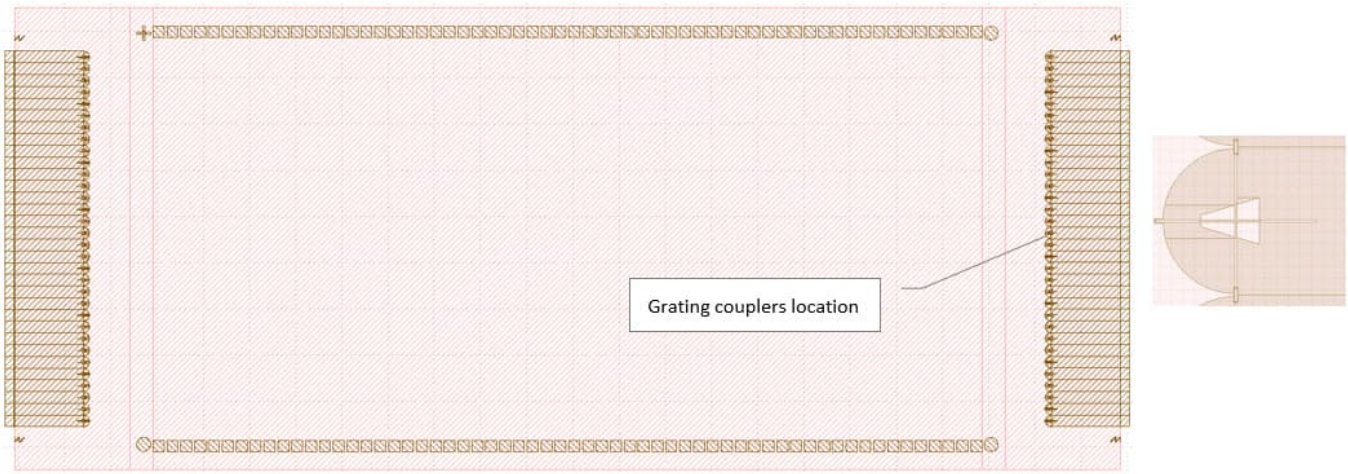

Figure 26: Example of a GDS file for grating coupling